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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
SORRELL, ERON J

ART UNIT	PAPER NUMBER
2182	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/932,330	HUPPENTHAL ET AL.	
	Examiner	Art Unit	
	Eron J. Sorrell	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Appeal Brief

1. In view of the Appeal Brief filed on 2/9/07, PROSECUTION IS HEREBY REOPENED. New grounds of rejections are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

Response to Declaration filed under 37 CFR 1.132

2. Appellants declaration filed 2/9/07 has been fully considered and appears to be "expert analysis" regarding the combination of prior art references of US Patent 6,052,134 to Foster and US Patent 4,972,457 to O'Sullivan. Since this

combination is no longer relied upon in the new grounds of rejection, the arguments presented in the declaration are moot.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1,2,5-7,9-14,17-19, and 21-24 are rejected under 35 U.S.C. 102(a) as being anticipated by Klingelhofer (U.S. Patent No. 5,673,204).

5. Referring to claims 1 and 13, Klingelhofer teaches a computer system comprising:

at least one processor (item 40, figure 1);

a controller (item 90, figure 1) for coupling said at least one processor to a peripheral bus control block (graphics control block) (item 100, figure 1) and a memory module bus (item 60, figure 1);

at least one peripheral bus slot (graphics bus connection) coupled to said peripheral bus control block by a peripheral bus (graphics bus) (see lines 26-44 of column 3);

at least one memory module slot coupled to said memory module bus (see item 70, figure 1, note the SIMMs sit in slots); and

a processor element (item DX, figure 1, and lines 39-44 of column 3) associated with said at least one memory module slot for providing a direct data connection between an external device coupled thereto and the memory module slot enabling data exchange directly between the external device and the memory module bus (see lines 7-18 of column 4, note the IOSIMM provides a direct connection between the video adapter and the memory module bus).

6. Referring to claims 2 and 14, Klingelhofer teaches the computer system further comprising a control connection to said processor element (see item 360 in figure 2, and its connection to the bus) coupled to said peripheral bus for indicating to said at least one processor an arrival of data on said direct data connection to said processor element and memory module bus (see lines 30-38 of column 8).

7. Referring to claims 5,6,17, and 18, Klingelhofer teaches the memory module bus comprises a in-line memory module serial interface bus (see item 60, figure 1) and the processor element comprises an in-line memory module physical format for retention with the serial bus (see lines 6-18 of column 4).

8. Referring to claims 7 and 19, Klingelhofer teaches the external device may be another computer system (see paragraph bridging columns 3 and 4).

9. Referring to claims 9 and 21, Klingelhofer teaches the processor element is operative to alter data received from the external device prior to transmission on the memory module bus (see lines 20-26 of column 5, note the bi-directional communication links).

10. Referring to claims 10 and 22, Klingelhofer teaches the processor element is operative to alter data received from the external device prior to transmission on the memory module bus (see lines 20-26 of column 5).

11. Referring to claims 11 and 23, Klingelhofer teaches the processor element can be implemented as an FPGA (see lines 20-26 of column 5).

12. Referring to claims 12 and 24, Foster teaches implementing a processor as a plurality of processors (see lines 13-36 of column 1).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Klingelhofer with the above teachings of Foster to increase the processing power of the system.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 3,4,8, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klingelhofer in view of Foster (U.S. Patent No. 6,052,134).

15. Referring to claims 3 and 4, Klingelhofer teaches the system of claims 1 and 13, as shown above, however Klingelhofer fails to teach the memory module bus is a DIMM bus and that the processor elements has a DIMM physical format, however Klingelhofer does teach a SIMM bus and a SIMM physical format (see item 60, figure 1).

Foster teaches a typical computer system, wherein the memory bus is a DIMM bus and the slots require a DIMM physical format (see paragraph bridging columns 6 and 7; Note DIMMs have a 64-bit width and Foster discloses the memory banks disclosed have a 64-bit width).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Klingelhofer with the above teachings of Foster because DIMMs have a wider bus width allowing for more storage capacity and can added to the system individually instead of by pairs as required with SIMMs.

16. Referring to claim 8 and 20, Foster teaches that typical computer systems comprise a PCI bus and an AGP bus (see item labeled PCI, and AGP in figure 1).

It would have been obvious to one of ordinary skill in the art at the time of the applicants invention to modify the system of Klingelhofer with the above teachings of Foster because the PCI bus is used in most typical computer systems and has a high data transfer rate between the peripheral and the graphics bus and the CPU and.

17. Claims 25-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klingelhofer in view of Whittaker et al. (U.S. Patent No. 5,889,959 hereinafter "Whittaker").

18. Referring to claim 25, Klingelhofer teaches a computer system comprising:

at least one processor (item 40, figure 1);

a controller (item 90, figure 1) for coupling said at least one processor to control block (item 100, figure 1) and a memory module bus (item 60, figure 1);

at least one memory module slot coupled to said memory module bus (see item 70, figure 1, note the SIMMs sit in slots); and

a processor element (item DX, figure 1, and lines 39-44 of column 3) associated with said at least one memory module slot for providing a direct data connection between an external

device coupled thereto and the memory module slot enabling data exchange directly between the external device and the memory module bus (see lines 7-18 of column 4, note the IOSIMM provides a direct connection between the video adapter and the memory module bus).

Klingelhofer fails to teach a system maintenance control block with a connection to a system maintenance control bus.

Whittaker teaches a control block comprising a systems maintenance control block, wherein the systems maintenance control block provides control information processor element over a system maintenance bus (see lines 42-49 of column 4).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Klingelhofer with the above teachings of Whittaker. One of ordinary skill in the art would have been motivated to make such modification in order to provide diagnostic functions to all of the modules in the system as suggested by Whittaker (see lines 30-43 of column 1).

19. Referring to claim 26, Klingelhofer teaches the computer system further comprising a control connection to said processor element (see item 360 in figure 2, and its connection to the bus) coupled to said peripheral bus for indicating to said at

least one processor an arrival of data on said direct data connection to said processor element and memory module bus (see lines 30-38 of column 8).

20. Referring to claims 29 and 30, Klingelhofer teaches the memory module bus comprises an in-line memory module serial interface bus (see item 60, figure 1) and the processor element comprises an in-line memory module physical format for retention with the serial bus (see lines 6-18 of column 4).

21. Referring to claim 31, Klingelhofer teaches the external device may be another computer system (see paragraph bridging columns 3 and 4).

22. Referring to claim 32, Whittaker teaches the bus is an SM Bus (see lines 42-49 of column 4). It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Klingelhofer with the teachings of Whittaker for the same reasons as mentioned above.

23. Referring to claim 33, Klingelhofer teaches the processor element is operative to alter data received from the external

device prior to transmission on the memory module bus (see lines 20-26 of column 5, note the bi-directional communication links).

24. Referring to claim 34, Klingelhofer teaches the processor element is operative to alter data received from the external device prior to transmission on the memory module bus (see lines 20-26 of column 5).

25. Referring to claims 35, Klingelhofer teaches the processor element can be implemented as an FPGA (see lines 20-26 of column 5).

26. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Klingelhofer in view of Whittaker as applied to claim 25 and further in view of Foster.

27. Referring to claim 36, the combination of Klingelhofer and Whittaker teaches the system of claim 25, however the combination fails to teach the processor being implemented as a plurality of processors, Foster teaches implementing a processor as a plurality of processors (see lines 13-36 of column 1).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the

system of Klingelhofer with the above teachings of Foster to increase the processing power of the system.

Conclusion

28. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following document is cited to further show the state of the art as it pertains to the applicant's invention:

Fiscal 1994 Project Portfolio Report discloses the concept of connecting I/O devices directly to the system memory bus.

29. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eron J. Sorrell whose telephone number is 571 272-4160. The examiner can normally be reached on Monday-Friday 8:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KIM HUYNH
SUPERVISORY PATENT EXAMINER
6/8/07